



10/701165

cfc.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 7,187,038 B2 )  
MORIN ET AL. )

Issued: March 6, 2007 )

For: SEMICONDUCTOR DEVICE WITH MOS )  
TRANSISTORS WITH AN ETCH-STOP LAYER )  
HAVING AN IMPROVED RESIDUAL STRESS )  
LEVEL AND METHOD FOR FABRICATING )  
SUCH A SEMICONDUCTOR DEVICE )

REQUEST FOR CERTIFICATE OF CORRECTION OF  
OFFICE MISTAKE UNDER RULE 1.322(a)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Certificate  
JUN 29 2007  
of Correction

Sir:

In accordance with the provisions of Rule 1.322(a) of the Rules of Practice, the Patent Office is respectfully requested to correct matters in the above-identified patent in accordance with the Certificate of Correction Form PTO-1050 attached hereto.

The Patent Office is requested to issue a Certificate of Correction on the above-referenced Patent Document, and to place such a Certificate of Correction in the file, so that such will appear on any copies of the patent which are ordered in the future.

The corrections being made are of consequence to provide the proper recitation in the claims. Moreover, since these errors are believed to be errors of the Patent Office, such

JUN 29 2007

In re Patent of  
**MORIN ET AL.**  
Patent No. 7,187,038 B2  
Issued: **March 6, 2007**

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changes should be made at no expense to the Patentee. No new matter is added by these corrections.

Respectfully submitted,

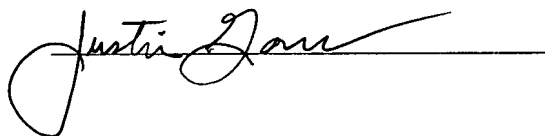


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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22<sup>nd</sup> day of June, 2007.



JUN 29 2007

**UNITED STATES PATENT AND TRADEMARK OFFICE**

**CERTIFICATE OF CORRECTION**

PATENT NO.	:	7,187,038 B2
DATED	:	March 6, 2006
INVENTOR(S)	:	Morin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

Column 6, Line 20

Delete: "NMOS transistor and the at least one transistor;"  
Insert: --PMOS transistor and the at least one NMOS  
transistor;--

MAILING ADDRESS OF SENDER:

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